In the Claims:

Please amend claim 3 -11. Please cancel claims 1 and 2. The claims are as follows:

1-2 (Canceled)

3. (Currently Amended) [[The]] A structure ~~of claim 2, further~~ including:

a substrate having a top surface, said substrate of a first dopant type;

a first semiconductor layer in said substrate, said first semiconductor layer having a top surface extending parallel to said top surface of said substrate, said first layer of a second dopant type; and

a second semiconductor layer of said first dopant type, said second semiconductor layer having a top surface coextensive with said top surface of said substrate, a bottom surface of said second layer in direct physical contact with said top surface of said first layer, said second layer electrically modulated by said first layer;

a source and a drain of said first dopant type in said second layer and a gate formed on said top surface of said substrate and aligned to said source and said drain;

a first vertical bipolar transistor comprising said source, said second semiconductor layer and said semiconductor first layer; and

a second vertical bipolar transistor comprising said drain, said second semiconductor layer and said first semiconductor layer; and

a third ~~horizontal~~ semiconductor layer of said second dopant type ~~on top of and~~ a bottom surface of said third semiconductor layer in direct physical contact with said top surface of said first semiconductor layer and extending ~~vertically~~ in a direction perpendicular to said top surface

of said substrate into said ~~first~~ second semiconductor layer, said second layer further electrically modulated by said third semiconductor layer.

4. (Currently Amended) The structure of claim 3, wherein said third semiconductor layer extends horizontally ~~under~~ parallel to said top surface of said substrate in said second semiconductor layer between said source, said drain and said gate and said first semiconductor layer.

5. (Currently Amended) The structure of claim 3, further including:

a contact to said second semiconductor layer formed in said second semiconductor layer and extending perpendicular to said top surface of said substrate into said second semiconductor layer;

a shallow trench dielectric isolation formed in said second semiconductor layer, said shallow trench dielectric isolation extending from said top surface of said substrate perpendicular to said top surface of said substrate into said second semiconductor layer; and

wherein said third semiconductor layer extends ~~horizontally under~~ parallel to said top surface of said substrate in said second semiconductor layer between said second semiconductor layer and said [[a]] shallow trench dielectric isolation ~~formed between said source or said drain and a contact to said second layer~~.

6. (Currently Amended) The structure of claim 3, further including:

a contact to said second semiconductor layer formed in said second layer and extending perpendicular to said top surface of said substrate into said second semiconductor layer; and

wherein said third semiconductor layer extends ~~horizontally under~~ parallel to said top surface of said substrate in said second semiconductor layer between said ~~under~~ a contact to said second semiconductor layer and said first semiconductor layer.

7. (Currently Amended) The structure of claim [[2]] 3, further including:

vertical isolation comprising shallow trench dielectric isolation in combination with deep trench dielectric isolation, trench dielectric isolation or diffused isolation;

said vertical isolation extending ~~vertically~~ perpendicular to said top surface of said substrate from said top surface of said substrate into or past said first semiconductor layer and isolating said second semiconductor layer.

8. (Currently Amended) The structure of claim [[1]] 3, further including:

multiple fingers of source, multiple fingers of drain or multiple fingers of both source and drain a gate formed on said top surface of said substrate and aligned to said source and drain fingers;

one or more vertical bipolar transistors each comprising one source finger, said second layer and said first semiconductor layer; and

one or more vertical bipolar transistors each comprising one drain finger, said second layer and said first semiconductor layer.

9. (Currently Amended) The structure of claim [[1]] 3, wherein said third semiconductor layer comprises a collector of a bipolar transistor and said first ~~horizontal~~ semiconductor layer ~~is the same as~~ comprises a subcollector of [[a]] said bipolar transistor formed in said substrate.

10. (Currently Amended) The structure of claim [[1]] 3, wherein said first dopant type is P-type and said second dopant type is N-type.

11. (Currently Amended) The structure of claim [[1]] 3, wherein said second semiconductor layer comprises epitaxial silicon.

12. (Withdrawn) A trigger device comprising:

a lateral MOSFET comprising a source, a drain, a gate and a body;

a modulating layer under and in contact with said body;

a first vertical bipolar transistor comprising said source, said body and said modulating layer; and

a second vertical bipolar transistor comprising said drain, said body and said modulating layer.

13. (Withdrawn) The trigger device of claim 12, further including means for lateral isolation of said source, said drain and said body.

14. (Withdrawn) The trigger device of claim 12, further including a modulator extension, in electrical contact with and extending vertically from said modulator into said body.

15. (Withdrawn) The trigger device of claim 12, wherein said source, said drain or both said source and said drain comprise multiple fingers and said first vertical bipolar transistor, said

second vertical bipolar transistor or both said first and second vertical bipolar transistors comprise multiple bipolar transistors, one vertical bipolar transistor for each source finger and one vertical bipolar transistor for each drain finger.

16. (Withdrawn) The trigger device of claim 12, wherein application of a bias to said modulator decreases a gate voltage at which MOSFET breakdown occurs.

17. (Withdrawn) A method of electrostatic discharge protection, comprising:

providing trigger device comprising:

a MOSFET having a source, a drain, a gate and a body in a substrate;

a modulator under and in contact with said body;

a first vertical bipolar transistor comprising said source, body and modulator; and

a second vertical bipolar transistor comprising said drain, body and modulator;

coupling said modulator to said substrate and to an I/O pad; and

coupling said modulator and said drain to an input gate, to a double gated diode pair and input gate network or to a clamping network.

18. (Withdrawn) The method of claim 18, further including, applying a bias voltage to said modulator to change the forward biases on said first and second vertical bipolar transistors.

19. (Withdrawn) The method claim 17, further including, applying a bias voltage to said modulator to change the lateral resistance of said body.

20. (Withdrawn) The method of claim 17, further including coupling said gate and said source to ground.